**ASSIGNMENT-2**

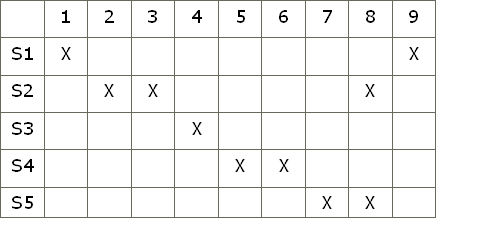
1. Discuss the classification of pipelined processor based on
   1. levels of processing and
   2. the pipeline configuration and control strategies

Draw the appropriate diagrams while discussing the classification.

1. i) Define the following with respect to pipelining:
2. Evaluation Time b) Latency Cycle c) Reservation Table

ii) Consider the RT shown:

1. Det latencies in the forbidden list, F and the collision vector, C
2. Draw the state transition diagram
3. List all Latency cycles, Simple cycles and Greedy cycles.
4. Det MAL.
5. Determine the η of given pipeline.
6. If clock period, ґ = 20ns, det the maximum throughput of the pipeline.
7. Determine the throughput of the pipeline for obtained η.



1. ii) A processor is nonpipelined and has a clock rate of 25MHz. It has average CPI of 4. Two more processors A and B has clock rate of 20MHz each where processor A is designed with 5 stages and processor B with 9 stages. A program has 1000 instructions to be executed. What is the speedup of each pipelined over nonpipelined? Also find MIPS rate of each processor during execution of the pgm?
2. Define the following with respect to pipelining:
3. Collision vector b) State Transition diagram c) Permissible latency
4. Define instruction level parallelism. Give the equation for pipeline CPI considering various pipeline stalls. Discuss all possible data hazards considering two instructions *i* and *j*, with *j* occurring before *i* in program order.
5. Considering appropriate assembly language program segment do a detailed discussion on control dependency.